UNITED STATES PATENT AND TRADEMARK OFFICE **CERTIFICATE OF CORRECTION**

PATENT NO.

: 6,819,611 B2

Page 1 of 1

APPLICATION NO. : 09/964113

DATED

: November 16, 2004

INVENTOR(S)

: Brent Keeth

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title Page,	Reads	Should Read
Item (56), References Cited, Other Publications	"Descriptive literature entitled, 400MHz SLDRAM, 4Mx16 SLDRAM Piplined, Eight Bank, 2.5 V Operation, SLDRAM Consortium Advance Sheet, published throughout the United	Descriptive literature entitled, "400MHz SLDRAM, 4Mx16 SLDRAM Pipelined, Eight Bank, 2.5 V Operation," SLDRAM Consortium Advance Sheet, published throughout the United
Title Page,	States, pp. 1-22."	States, pp. 1-22."
Item (57), Line 1	"pair of arrays"	pair of arrays,
Column 4, Line 23	"November. 1991 and"	November 1991 and
Column 7, Line 62	"appended claims. which"	appended claims, which
Column 8, Line 28	"gate of a transistor"	gate of a transistor;
Column 9, Line 5	"columns each colunn"	columns, each column
Column 9, Line 16	"complementary dais lines"	complementary data lines
Column 9, Line 57	"coupled a"	coupled to a
Column 10, Line 48	"and in"	and an
Column 11, Line 32	"transistor"	transistor;
Column 12, Line 41	"logic stare"	logic state

Signed and Sealed this

Twenty-eighth Day of November, 2006

JON W. DUDAS Director of the United States Patent and Trademark Office